American Public University System
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CSCI350 : Digital Systems II

Course Summary

Course: CSCI350 Title: Digital Systems II

Length of Course: 16

Prerequisites: CSCI150 Credit Hours: 3

Description

Course Description:

This course advances the student's understanding of PDLs, FPGA design flows, and ability to perform HDL-based design and implementation on FPGAs. Students learn to design, synthesize, simulate, and implement logic on an actual device, as well as understand and work with FPGA architectures, digital arithmetic, pipelining, and parallelism. Students will become knowledgeable to make a substantial modification to a simple microcontroller-based system and identify the cyber concerns associated with it. The course provides hands-on training on the use of a hardware-description language. In addition, students will be able to detect failures in security design principles, and how they can lead to system vulnerabilities that can be exploited as part of an offensive cyber operation.

Course Scope:

The course starts with a review of and digital systems and switching circuits. The course then moves into binary arithmetic, sign and magnitude numbers, 2's complement numbers, addition of 2's complement numbers followed by an introduction to Boolean Algebra, Karnaugh Maps, Quine-McCluskey Method, multi-Level Gate Circuits NAND and NOR Gates. The course then progresses into combinational circuit design, multiplexers, decoders, programmable logic devices and an introduction to Latches, Flip-Flops and an introduction to registers and counters. FPGA design flaws are introduced and students learn HDL-based design and learn to work with FPGA architectures. The course then dives into design controls implemented in industrial applications, and the best modeling and identification techniques for dynamic systems are presented and explained for system security vulnerabilities. Labs on how to secure a Raspberry Pi follows and ends with analysis of clocked sequential circuits.

Objectives

By the end of this course, you will be able to:

- CO1: Apply advanced Boolean Algebra expressions in digital systems and switching circuits.
- CO2: Analyze various methods such as Quine-McCluskey, K-Maps, and Petrick's to minimize the Boolean expression.
- CO3: Analyze circuits containing multiplexers, decoders, and programmable logic devices.

- CO4: Evaluate differences between VHDL, Latches, and Flip-flops.
- CO5: Construct programs using various programming languages.
- CO6: Compare various system security design flaws that can lead to system vulnerabilities.
- CO7: Classify programmable architectures in digital system designs.
- CO8: Explain the concepts of Memory Management, pipeline, and Parallelism in Digital Systems.

Outline

Week 1: Definition and Introduction to Digital Systems

Learning Outcomes

CO-1: Apply advanced Boolean Algebra expressions in digital systems and switching circuits. circuits.

LO-1.1: Compare combinational logic circuits such as AND gate, OR gate, NOT gate, and the exclusive XOR gate.

LO-1.2: Formulate Octal to Decimal Conversions.

LO-1.3: Implement Radix Multiplication.

LO-1.4: Explain Gray Code to Binary Conversions.

Assignments

- Week 1 Welcome Discussion – For week 1, the discussion is due at the end of the week on Sunday. In subsequent weeks, the initial post is due mid-week. (ungraded but required)
- Week 1: Chapter Review Problems
- Week 1 Assignment 1: Number Base Conversion using Python

Week 2: Review of Boolean Algebra

Learning Outcomes

CO-1: Apply advanced Boolean Algebra expressions in digital systems and switching circuits.

LO-1.5: Explain constants and variables used in logic design.

LO-1.6: Implement basic Truth Tables using gate operators.

LO-1.7: Describe basic and advanced gate operators and logic gate designs.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 2: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Read: Chapters 2 & 3: Digital Systems Design: Volume 1

Assignments

Week 2 Discussion: Differences Between AND gates, OR gates, and Inverters

Week 2 Chapter Review Problems

Week 3: Karnaugh Maps-Logic Circuits

Learning Outcomes

CO-1: Apply advanced Boolean Algebra expressions in digital systems and switching circuits.

LO-1.8: Construct Boolean Algebra symbology and logic operators.

LO-1.9: Formulate Theorems implementing and interpreting truth tables.

LO-1.10: Compare a series of rules used to find minterms and maxterms.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 4: Fundamentals of Logic Design, Enhanced Edition, 7th Edition.

Read: Chapter 4: Digital Systems Design: Volume 1

Assignments

Week 3 Discussion: K-Maps

Week 3 Chapter Review Problems

Week 4: Quine-McCluskey Method

Learning Outcomes

CO2: Analyze various methods such as Quine-McCluskey, K-Maps, and Petrick's to minimize the Boolean expression.

LO-2.1: Evaluate the Quine-McCluskey method against Karnaugh maps.

LO-2.2: Analyze data to find all prime implicants of the function.

LO-2.3: Construct a systematic simplification procedure to reduce a minterm.

LO-2.4: Compare Implicants and prime implicants against K-Map.

LO-2.5: Design Two-level simplifications using Karnaugh Maps.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 6: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Read: Chapter 1: Digital Systems Design: Volume 2

Assignments

Week 4 Discussion: Quine-McCluskey Method

Week 4 Chapter Review Problems

Week 5: NAND and NOR Gates

Learning Outcomes

CO3: Analyze circuits containing multiplexers, decoders, and programmable logic devices.

- LO-3.1: Design Multi-level gate circuits.
- LO-3.2: Analyze the differences between NAND and NOR gates circuits.
- LO-3.3: Compare Two-level and Multi-Level NAND and NOR gates.
- LO-3.4: Convert circuits by adding or deleting inversion bubbles.
- LO-3.5: Demonstrate circuit conversion using alternative gate symbols.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 7: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Read: Chapter 2: Digital Systems Design: Volume 2

Assignments

Week 5 Discussion: NAND and NOR Gates

Week 5 Chapter Review Problems

Week 6: VHDL Statements and Combinational Logic

Learning Outcomes

CO-4: Evaluate differences between VHDL, Latches, and Flip-flops.

- LO-4.1: Formulate Boolean Algebra for digital circuits using reduction, expansion, and factoring.
- LO-4.2: Assess IEEE Standard 1076 VHDL Hardware Description Language
- LO-4.3: Design, debug, and simulate digital systems using VHDL.
- LO-4.4: Synthesize complex digital circuits at several levels of abstraction.
- LO-4.5: Analyze and implement logic on FPGA and CPLD.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 10: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Read: Chapter 3: Digital Systems Design: Volume 2

Assignments

Week 6 Discussion: VHDL and CPLD Statements

Week 6 Chapter Review Problems

Week 7: Mid-Term Exam

Learning Outcomes

Course Objective(s)

The mid-term exam will assess the following course objectives.

CO1: Apply advanced Boolean Algebra expressions in digital systems and switching circuits.

CO2:Analyze various methods such as Quine-McCluskey, K-Maps, and Petrick's to minimize the Boolean expression.

CO3: Analyze circuits containing multiplexers, decoders, and programmable logical devices.

CO4: Evaluate differences between VHDL, Latches, and Flip-flops.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

No readings this week, you will review all prior weeks as you prepare for your mid-term.

Assignments

Week 7 Discussion: Interesting Topics from Weeks 1-6 (ungraded)

Mid-Term Exam

Week 8: Latches and Flip-Flops

Learning Outcomes

CO-4: Evaluate differences between Latches and Flip-flops.

LO-4.6: Compare differences between S-R and gated D latches.

LO-4.7: Create timing diagrams relating to input and output of such latches and flip-flops.

LO-4.8: Design latches and flip-flops using gates.

LO-4.9: Analyze the operation of a flip-flop that is constructed of gates and latches.

LO-4.10: Design a S-R latch using NOR gates.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 11: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Read: Chapter 1(pages 1-29): Digital Systems Design: Volume 3

Assignments

Week 8 Discussion: Latches

Week 8 Chapter Review Problems

Week 9: Operation of Registers

Learning Outcomes

CO-4: Evaluate differences between Latches and Flip-flops.

LO-4.11: Analyze the operation of registers and how they transfer data between registers using a tri-state bus.

LO-4.12: Evaluate the operation of shift registers.

LO-4.13: Design shift registers using flip-flops.

LO-4.14: Arrange desired counting sequence for a counter.

LO-4.15: Construct a timing diagram for a counter by tracing signals through the circuit.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 12: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Read: Chapter 1(Pages 29-63): Digital Systems Design: Volume 3

Assignments

Week 9 Discussion: Simple Data Path Application Design

Week 9 Chapter Review Problems

Week 10: Characteristics of Digital Circuits

Learning Outcomes

CO-7: Classify programmable architectures in digital system designs.

LO-7.1: Explain the Characteristics of Digital Circuits.

LO-7.2: Analyze RC Time Constant.

LO-7.3: Summarize Electrical Behavior of Circuits.

LO-7.4: Explain Circuit Behavior With Circuit Loads.

LO-7.5: Analyze what sequences or groups of sequences must be remembered by the circuit and set up states accordingly.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 14: Fundamentals of Logic Design, Enhanced Edition, 7th Edition
Read: Chapter 2(Pages 79-120): Digital Systems Design: Volume 3

Assignments

Week 10 Discussion: Sequential Circuits

Week 10 Chapter Review Problems

Week 11: Reduction of State Tables

Learning Outcomes

CO-7: Classify programmable architectures in digital system designs.

LO-7.6: Differentiate equivalent states, state several ways of testing for state equivalence, and determine if two states are equivalent.

LO-7.7: Construct equivalent sequential circuits and determine if two circuits are equivalent.

LO-7.8: Evaluate a state table and assignment, form the transition table and derive flip-flop input equations.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read Unit 15: Fundamentals of Logic Design, Enhanced Edition, 7th Edition.

Read: Chapter 2 (Pages 79-120): Digital Systems Design: Volume 3

Assignments

Week 11 Discussion: State Tables

Week 11 Chapter Review Problems

Week 12: VHDL for Sequential Logic

Learning Outcomes

CO-7: Classify programmable architectures in digital system designs.

LO-7.9: Construct flip-flops, shift registers, and counters using VHDL processes..

LO-7.10: Develop sequential VHDL statements, including if-then-else, case, and wait statements.

LO-7.11: Analyze VHDL code for sequential logic, draw the corresponding logic circuit.

LO-7.12: Design, simulate, and synthesize a sequential logic module.

LO-7.13: Analyze how flip-flops change state on the same clock edge.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 17: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Assignments

Week 12 Discussion: Combinational and Sequential logic in VHDL

Week 12 Assignment: Programming in C

Week 13: Design System using VHDL

Learning Outcomes

CO-5: Construct programs using various programming languages.

LO-5.1: Synthesizable VHDL code for the system using control signals.

LO-5.2: Design a VHDL test bench to test a VHDL module.

LO-5.3: Differentiate block diagrams and a state graphs for a digital systems.

LO-5.4: Evaluate combinational logic for updating registers.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Unit 20: Fundamentals of Logic Design, Enhanced Edition, 7th Edition

Assignments

Week 13 Discussion: Poorly written codes

Week 13 Interactive Assignment

Week 14: Memory Management

Learning Outcomes

CO-8: Apply pipelining and parallelism using step modules and multiplexer to pass data.

LO-8.1: Demonstrate various techniques such as pipeline, Parallelism, and memory management.
LO-8.2: Compare memory hierarchy with cache architecture to reduce memory access latency to support hardware performance
LO-8.3: Explain the RISC Processor

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Chapter 4: Computer organization and design: the hardware/software interface Patterson, David A ; Hennessy, John L 2017

Read: Chapter 6: FPGA Programming for Beginners Frank Bruno, 2021

Assignments

Week 14 Discussion: Memory Management

Week 15: Digital System Security Design Flaws and Vulnerabilities

Learning Outcomes

CO-6: Compare various system security design flaws that can lead to system vulnerabilities.

LO-6.1: Evaluate security in digital architecture.

LO-6.2: Compare various threat models.

LO-6.3: Develop rules to minimize security design flaws.

LO-6.4: Construct detection guidelines to detect vulnerabilities.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

Read: Frontiers of Engineering: Reports on Leading-Edge Engineering from the 2015 Symposium

Assignments

Week 15 Discussion: System security design flaws

Week 16: Retrospective & Final Exam

Learning Outcomes

CO5: Construct programs using various programming languages.

CO6: Compare various system security design flaws that can lead to system vulnerabilities.

CO7: Classify programmable architectures in digital system designs.

CO8: Explain the concept of Memory Management, pipeline, and Parallelism in Digital Systems.

Reading and Resources

Links for all readings are provided in the course e-reserve. This is located in each of the weekly lessons.

No readings this week, you will review all prior weeks as you prepare for your Final.

Assignments

Week 16 Discussion: Retrospective

Final Exam

Evaluation

Late Assignments

Students are expected to submit assignments by the due dates listed in the classroom. Late assignments, including but not limited to Assignments, Discussions, posts and responses, quizzes, and exams, may or may not be accepted after the course end date. Submitting an assignment after the due date may result in a penalty of up to 10% of the grade per day late, not to exceed a maximum 50% of the grade. The amount of the penalty is at the faculty member's discretion. Faculty recognize that students have limited time and maybe more flexible if potential delays are communicated ahead of time.*

*Doctoral and Programs with specialty accreditation may have different late policies.

**Students with DSA accommodations may have different late policies applied. For more information regarding our DSA services, please contact DSA@apus.edu.

Grading

Name	*Grade %*
Discussions	**20%**
Assignments	**30%**
Chapter Review Questions	20 %
Programming Assignments	10%
Exams	**50%**
Mid-Term	25%
Final Exam	25%
Total	**100%**

Materials

Book Title: Various resources from Trefry Library and/or the Open Web are used. Links provided inside the classroom.

All required readings are located in the Reading and Resources tab under the Lessons tab.

Fundamentals of Logic Design, Enhanced Edition, 7th Edition.

Digital Systems Design: Volume 1

Digital Systems Design: Volume 2

Digital Systems Design: Volume 3

Computer organization and design: the hardware/software interface Patterson, David A ; Hennessy, John L 2017

FPGA Programming for Beginners Frank Bruno, 2021

Frontiers of Engineering: Reports on Leading-Edge Engineering from the 2015 Symposium

Course Guidelines

Writing Expectations

All activities completed in this course are to follow the stated instructions (inside the classroom). Always check the grading rubrics to see what your instructor will be on the lookout for when grading your work. Also, be sure you have read the APUS Plagiarism Policy (the entire Academic Dishonesty section) before submitting work in this or in any other course. See the above Course Outline or the Policies section on this Syllabus for links.

Citation and Reference Style

Attention: You will follow the citation style that is common to your discipline. Instructions regarding citation styles are included in the classroom.

Late Assignments

Students are expected to submit assignments by the due dates listed in the classroom. Late assignments, including but not limited to Assignments, Discussions, posts and responses, quizzes, and exams, may or may not be accepted after the course end date. Submitting an assignment after the due date may result in a penalty of up to 10% of the grade per day late, not to exceed a maximum 50% of the grade. The amount of the penalty is at the faculty member's discretion. Faculty recognize that students have limited time and maybe more flexible if potential delays are communicated ahead of time.*

*Doctoral and Programs with specialty accreditation may have different late policies.

**Students with DSA accommodations may have different late policies applied. For more information regarding our DSA services, please contact DSA@apus.edu.

Also, completing all Assignments (under the Assignments tab) is paramount to your success in this course.

Netiquette

Online universities promote the advancement of knowledge through positive and constructive debate, both inside and outside the classroom. Forums on the Internet, however, can occasionally degenerate into needless insults and flaming. Such activity and the loss of good manners are not acceptable in a university setting. Basic academic rules of good behavior and proper Netiquette must persist. Remember that you are in a place for the rewards and excitement of learning, which does not include descent to personal attacks orstudent attempts to stifle the learning of others.

- Humor Note: Despite the best of intentions, jokes and especially satire can easily get lost or taken seriously. If you feel the need for humor, you may wish to add emoticons to help alert your readers: ;-), :), .

Disclaimer Statement

Course content may vary from the outline to meet the needs of this particular group.

Communications

Student Communication

To reach the instructor, please communicate through the MyClassroom email function accessible from the Classlist of the Course Tools menu, where the instructor and students email addresses are listed, or via the Office 365 tool on the Course homepage.

- In emails to instructors, it's important to note the specific course in which you are enrolled. The name of the course is at the top center of all pages.
- Students and instructors communicate in Discussion posts and other learning activities.
- All interactions should follow APUS guidelines, as noted in the Student Handbook, and maintain a professional, courteous tone.
- Students should review writing for spelling and grammar.
- Tips on Using the Office 365 Email Tool

Instructor Communication

The instructor will post announcements on communications preferences involving email and Instant Messaging and any changes in the class schedule or activities.

- Instructors will periodically post information on the expectations of students and will provide feedback on assignments, Discussion posts, quizzes, and exams.
- Instructors will generally acknowledge student communications within 24 hours and respond within 48hours, except in unusual circumstances (e.g., illness).

- The APUS standard for grading of all assessments (assignments, Discussions, quizzes, exams) is five days or fewer from the due date.
- Final course grades are submitted by faculty no later than seven days after the end date of the course or the end of the extension period.

University Policies

Consult the Student Handbook for processes and policies at APUS. Notable policies:

- Drop/Withdrawal Policy
- Extension Requests
- Academic Probation
- Appeals
- Academic Dishonesty / Plagiarism
- Disability Accommodations
- Student Deadlines
- Video Conference Policy

Mission

The mission of American Public University System is to provide high-quality higher education with emphasis on educating the nation's military and public service communities by offering respected, relevant, accessible, affordable, and student-focused online programs that prepare students for service and leadership in a diverse, global society.

Minimum Technology Requirements

- Please consult the catalog for the minimum hardware and software required for undergraduate and graduate courses.
- Although students are encouraged to use the Pulse mobile app with any course, please note that not all course work can be completed via a mobile device.

Disclaimers

- Please note that course content – and, thus, the syllabus – may change between when a student registers for a course and when the course starts.
- Course content may vary from the syllabus' schedule to meet the needs of a particular group.